REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed May 30, 2006. All pending claims remain unchanged as previously presented and new claims 17-22 are added. Reconsideration and allowance of the application and presently pending claims 1-22 are respectfully requested.

Claim Rejections-35 U.S.C. §103

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, Jr. et al. U.S. Patent No. 6,300,668 (hereinafter Miller), in view of Anderson, U.S. Patent No. 6,951,384 (hereinafter Anderson).

In response to the rejection thereto, Applicants traverse the rejections and submit claims 1-16, as previously presented, is neither taught, disclosed, nor suggested by Miller, Anderson, or any of the other cited references, taken alone or in combination, and thus should be allowed.

Specifically, with respect to claim 1, as previously presented, recites in parts:

A process of fabricating a high resistance CMOS resistor, comprising the steps of:

...

forming a p-well in a non-active area of said p-type silicon substrate;

...

forming a first p-field region into said p-well and a second p-field region into said n-well, wherein said second p-field region forms a CMOS resistor

...

forming a patterned BPSG layer as an intermetal dielectric layer to build two contact openings exposing a portion of said n-type contact region and said two p-type contact regions;

... (Emphasis added)

Applicants submit that such a process as set forth in claim 1, as previously presented, is novel and unobvious over Miller, Anderson, or any of the other cited references, taken alone or in combination, and should be allowable.

First of all, the cited references including Miller and Anderson, fails to teach, disclose, or suggest the step of "**forming a p-well in a non-active area of said p-type silicon substrate**" that is required by the present process as set forth in claim 1. Regarding this limitation, the Examiner contends "p-well as part of PMOS of CMOS process" (Page 2 of the current Office Action). However, Applicants submit that the Examiner fails to give evidence sufficiently reading on the limitation of such a step. Miller teaches an NMOS process and an n-well formed thereby. Although Miller also teaches, in an alternative embodiment, "the first dopant region 13 may be created with the same p+ ion-implantation step used to create PMOS source/drain diffusions and p+ guardbars to contact p-type diffused well (p-well) regions created in substrate 10 as part of a conventional p-well CMOS process flow" (Col. 3, lines 32-37), such a process is introduced as an alternative embodiment. In such a way, the NMOS process and the PMOS process can independently be performed to fabricate a resistor respectively, and the n-well and p-well thereof are not taught to be formed in association for fabricating the resistor. As such, Miller fails to teach a step of "forming a p-well in a non-active area of said p-type silicon substrate" in association with the previous step of "forming an n-well in said p-type silicon substrate". It is held that "[A]scertaining the differences between the prior art and the claims at issue requires interpreting the claim language, and considering both the invention and the prior

art references as a whole", MPEP §2141.02. Applicants submit that when considering in its entirety, the claimed invention is novel and unobvious over Miller or any of the other cited references.

Secondly, Applicants submit that the present invention as set forth in claim 1 is distinct from Miller, because the p-well of the present invention is required to be formed within a non-active area while the alternative p-well of Miller is formed in an active area instead.

Thirdly, Applicants submit that the Examiner fails to identify the counter items indicating the claimed elements of "the first p-field region" and the "second p-field region". Applicants submit that if the Examiner construe the counterdopant region 22 as a p-well, it should not be used read on any p-field region else, and *vice versa*.

Fourthly, the Examiner admitted that "Miller fails to disclose the formation of BPSG layer as an intermetal dielectric layer before forming the metal contacts" (Page 3 of the current Office Action). In order to set up an obviousness type rejection, the Examiner contributes that a BPSG layer used in such a way as well known in the art. Applicants hereby otherwise traverse the assertion that it is well known in the art that BPSG is formed as intermetal dielectric layer because BPSG exhibit low temperature flow properties. The Examiner fails to show that the corresponding properties of BPSG are well known at the time the invention is made, and the why should a material having such properties must be well known to be used as "an intermetal dielectric layer before forming the metal contacts" without impermissible hindsight.

As set forth in MPEP §2144.03 *C*, the Examiner is invited to give adequate evidence supporting the above challenged assertion.

For at least the foregoing reasons, the present process as set forth in claim 1 is neither taught, disclosed, nor suggested by Miller, Anderson, or any of the other cited references, taken alone or in combination. As such, claim 1 and its dependent claims 2-16 should be allowed over the cited references.

New Claims

Claims 17-22 have been newly added to further define and/or clarify the scope of the invention.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-22 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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